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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,891	12/19/2001	Gee Sung Chae	8733.495.00	8845

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EXAMINER	
DUONG, THOI V	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,891	CHAE, GEE SUNG	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-27* is/are allowed.

6)☒ Claim(s) *28-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the Amendment, Paper No. 8, filed August 26, 2002.

Accordingly, claim 18 was amended. Currently, claims 18-41 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 28-41 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa et al. (USPN 6,445,428 B1) in view of Kim (USPN 6,177,970 B1).

As shown in Figs. 5A-5E, Fujikawa discloses a method of fabricating a TFT comprising:

forming a gate electrode 22 on a substrate 21;

forming a gate insulating film 23, a semiconductor layer 24, an ohmic contact layer 26A, 26B, and a buffer layer 27a, 27d on the gate electrode;

forming a pixel electrode on the buffer layer;

forming source and drain electrodes 27b, 27e on the buffer layer; and

forming a passivation layer 28 on a surface of the substrate,

wherein the gate electrode includes aluminum (Al) (col. 9, lines 8-10),

wherein the buffer layer includes titanium (Ti) (col. 8, lines 11-25),

wherein the source and drain electrodes include aluminum (Al) (col. 8, lines 11-25),

wherein the pixel electrode includes indium tin oxide (col. 8, lines 47-51),

wherein the drain electrode is electrically connected with the pixel electrode,

wherein the gate electrode is deposited by a sputtering process (col. 9, lines 8-10),

wherein the gate electrode is patterned using photolithography (col. 10, lines 55-59),

wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are formed on the gate insulating film by a plasma enhanced chemical vapor deposition (PECVD) process, wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are patterned (col. 9, lines 15-32),

wherein the pixel electrode is formed by a sputtering process, wherein the pixel electrode is patterned (col. 9, lines 60-67), and

wherein the passivation layer is formed by a deposition process (col. 9, lines 54-59).

Fujikawa discloses all aspects of the instant invention as shown above except for forming a common electrode on the passivation layer. As shown in Fig. 2, Kim discloses a method for manufacturing an in-plane switching mode liquid crystal display (LCD) device comprising forming a pixel electrode 40 and a common electrode 310 on a passivation layer 80 to reduce the light leakage and to lower the driving voltage of the display (col. 1, lines 41-57). Thus, it would have been obvious to one having ordinary

skill in the art at the time the invention was made to modify the method of Fujikawa with the teaching of Kim by forming a common electrode on the passivation layer so as to prevent the light leakage and minimize the driving voltage of the display.

Response to Arguments

4. Applicant's arguments filed July 23, 2003 have been fully considered but they are not persuasive.

Applicant argued that Fujikawa and Kim fail to teach or suggest a method for manufacturing an in-plane switching mode LCD device comprising forming a pixel electrode on the buffer layer as recited in claim 28. The Examiner disagrees with the Applicant's remarks because, as clearly shown in Fig. 4 of Fujikawa, a gate insulating film 23, a semiconductor layer 24, an ohmic contact layer 26A, 26B, and a buffer layer 27a, 27d are formed on the gate electrode 22; and a pixel electrode 29 is formed on the buffer layer 27a, 27d. In addition, Kim's reference is employed for teaching forming a common electrode on the passivation layer to prevent the light leakage and minimize the driving voltage of the display.

Allowable Subject Matter

5. Claims 18-27 are allowed. (Note that these claims were previously allowed.)

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 18, none of the prior art of record discloses, in combination with other limitations as claimed, an in-plane switching mode liquid crystal display (LCD) device comprising:

a semiconductor layer and an ohmic contact layer on the gate insulating film;

a buffer layer on the ohmic contact layer;

a pixel electrode on the buffer layer;

source or drain electrodes connected with the pixel electrode on the buffer layer;

a passivation layer on the pixel electrode; and

a common electrode on the passivation layer.

The first most revelant reference, USPN 6,069,019 of Ishii et al., USPN 6,445,428 B1 of Fujikawa et al., and USPN 6,177,970 B1 of Kim, fail to disclose or suggest an in-plane switching mode liquid crystal display (LCD) device comprising, a pixel electrode formed on the buffer layer, a passivation layer on the pixel electrode, and a common electrode formed on the passivation layer. As shown in Figs. 8, 9 and 10B, the Ishii's reference discloses a LCD comprising a passivation layer 141 formed on a pixel electrode 129, but this pixel electrode 129 is formed under the buffer layer 139. Meanwhile, the Fujikawa et al.'s reference only discloses a pixel electrode 29 formed on the passivation layer 28 and the buffer layers 27a, 27d as shown in Fig. 4. And the Kim's reference only discloses a common electrode formed on the passivation layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong

10/01/2003

T. Chowdhury
Primary Examiner